Power System on a Chip (PSoC): Analog Emulation for Power System Applications

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Abstract-- **This contribution addresses VLSI-based hardware analog emulators of power systems. The goal is to develop a computational tool we refer to as a Power System on a Chip (PSoC). We review various problems and proposed solutions encountered from the design stage to the PC-board hardware implementation stage and finally to the anticipated VLSI implementation stage. In addition to various characteristic features, it has already been noted that using analog emulation for power system analysis allows for reduction in computation time, without significant loss in accuracy, compared to numerical methods. We further validate this through observations obtained from comparative runs between software and analog hardware environments.**

Index Terms-- **Analog computers, Analog processing circuits, Power system modeling, Power system simulation.**

I. INTRODUCTION

With current technology power-flow computation of large power systems is time intensive. There are numerous analog and digital computation methods currently utilized but they fail to meet the growing computational demands of power systems, particularly in system operations. The need to perform increasingly complex contingency studies and economic analyses on growing power grids is creating a tremendous computational burden. Traditional digital methods are too slow to solve the aforementioned demands quickly at a reasonable cost. Cluster computing is popular but the cost increases exponentially with the size of the system and the increase in computation performance does not increase at this same rate. Conversely, existing analog simulators can easily simulate the power system in real time, but consist of many analog components and require manual intervention to setup and configure the system for each calculation. Ideally, a real-time computation tool, or faster than real-time, is preferable.

Currently, digital simulation is the prevalent method for several reasons. These include i) the emergence of personal computers (PC) has made this technology reliable and easy to operate, and ii) advances in very large scale integration (VLSI) technology have allowed the development of new parallel computers with performance comparable to that of supercomputers at a fraction of the cost.

Typically, in digital simulation the set of algebraic expressions that describe power system behavior are discretized and software algorithms (such as Newton-Raphson) utilize input parameters to calculate the steady-state solution. For large-scale systems, studies are performed through the use of several types of massively parallel computers [1], [2]. The use of digital simulation analysis is seriously inhibited by lengthy computational times inherent to the iterative algorithms they employ.

An approach has arisen as to how analog technology may be utilized to perform analysis for larger power systems [3]. The main advantage of analog emulators is their shorter computational time. Within this rapidly growing area, several research foci exist.

- new reconfigurable analog tools such as operational transconductance amplifiers (OTA) and accompanying circuits
- component (generator, transmission line, load…) modeling both mathematical and circuit analogy
- control / data acquisition for large systems

The use of analog computational engines was quite widespread before digital technology reached the level of refinement and affordable price it has over the past thirty years. The idea of analog computation as a practical technology has been reintroduced by Fried et al. [3]. That work described how analog computational technology may be refined through advances in very large scale integration technology (VLSI). This paper will expand upon that work by outlining and reporting progress made on the necessary stages involved incorporating these advances. Because of the incorporation of VLSI technology in this approach, we propose the following name for the emulator; Power System on a Chip (PSoC).

Towards this end, PSoC development consists of building a programmable and reconfigurable analog mixed-signal circuit representation of a power network with complementary metal oxide semiconductor (CMOS) devices. The actual PSoC comprises a VLSI chip for simulation or emulation of its behavior. This emulator is initially designed for a steady-state load flow solver, which could be used for many applications. As will be shown this approach allows further study into circuit behavior with inclusion of power system dynamics. The success of this approach allows for ease of implementation and scaling into a VLSI chip.

The topic of this paper is presented in the following

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manner. In the next section, the problem formulation will describe the necessary stages involved in this research. Section III presents the methodology behind the modeling, simulation, printed circuit board (PCB) development and implementation of our analog emulator. In Section IV critical issues related to configuration, actuation and data acquisition are considered in order to justify speedup claims using this technique. Results presented in Section V will include a prototype of the proposed emulator with the goal of extracting system information and controlling various parameters and switches in order to accomplish the essential tasks required in emulating a small power system example. This will be followed by a discussions and conclusion.

II. PROBLEM FORMULATION

The development process involves four stages including feasibility studies, PCB design, VLSI design, and VLSI implementation as seen in Fig. 1.

Stage I focuses on the practicality of analog computation for power system studies avoiding development and construction of analog circuits and hardware. This is demonstrated with Analog Behavior Modeling (ABM) of electric circuits in PSpice that represents the power system and its behavior. This stage describes the intricacies of circuit connections and allows for model validation without any full structural design and implementation.

Stage II comprises development and realization of analog circuitry to replace the building blocks assembled in the previous stage. Using CMOS devices and software packages, the design, simulation, and PCB layout of power system components, i.e. generators, loads, transmission lines, etc, can be achieved. This development stage is broken up into two parts entailing circuit modeling and simulation and PC board development and emulation.

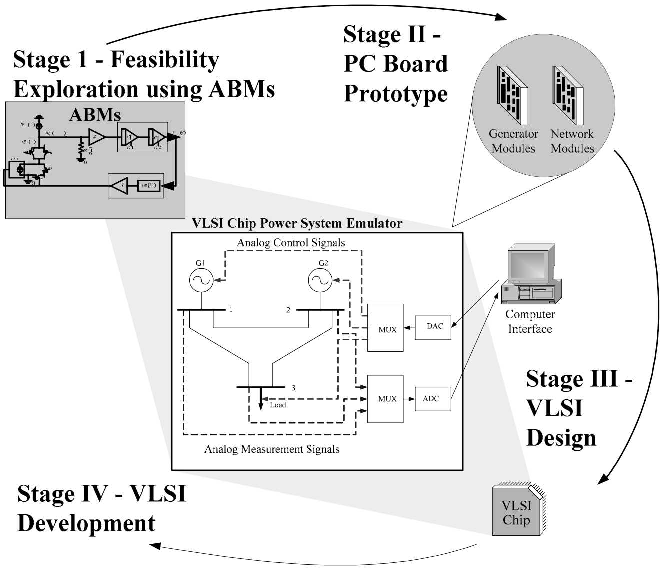

Fig. 1. PSoC Development Stages

Stages III and IV move this circuit realization into the final VLSI design and fabrication of a “Power System on a Chip”. Though not covered in this paper, we see similarities with the issues addressed in Stage II. These include modeling realizations of various power system components in addition to control and data acquisition schemes. The standout issue in these stages will be scalability issues involving system size capability and associated ramifications. The goal being to qualify and quantify what size power system can be captured on a given VLSI chip.

The next section details the background and systematic approach of each stage that was just described.

III. METHODOLOGY

A. Behavioral Modeling and Simulation

Power system component dynamic behavioral models consist of a set of algebraic/differential expressions. Before attempting to implement this relationship in analog hardware the exact form and complexity of these expressions must be defined as it dictates several characteristics of the resultant circuit. These include:

- the types and number of analog hardware control inputs and measurement outputs
- which parameters will be reconfigurable
- how the analog hardware will react to variations in the network state
- the size and complexity of the circuit

It is at this point the designer must decide what level of model complexity is appropriate for the intended use.

Once the mathematical component model has been finalized, it can be implemented into a circuit form using ABM components [4]. These ABM components only exist in simulation (within a software package such as PSpice) and provide ideal responses to external stimuli. They are immune to inaccuracies that plague real components such as signal noise, voltage/current offsets, operational errors, and finite operational ranges. The behavior of each ABM component, and the circuit as a whole, will later be approximated using real analog components. An example of a generator swing equation using ABM implementation is shown in Fig. 2.

$$M\ddot{\delta}+D\dot{\delta}+P_e(\delta)=P_m \Rightarrow$$

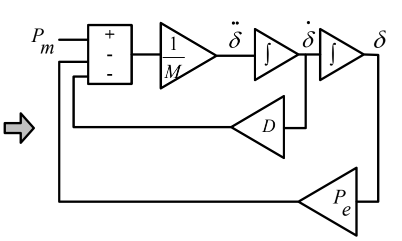

Fig. 2. Generator Swing Equation ABM Modeling Example

Hence, ABM models of power systems consist of ABM components and actual circuit elements such as resistors and sources interfacing one another seamlessly.

B. Circuit Modeling and Simulation

By developing ABM models, we have appropriate building blocks that can be implemented with analog circuitry. The circuit modeling and simulation stage is performed in software using commercially available electronic device macro-models. The key element of this research is the operational transconductance amplifier (OTA) [5]. The OTA is a voltage-controlled current source with an externally controlled gain. This extends the boundaries of basic op-amps and makes realizable designs that were previously unobtainable.

Since the OTA has externally controllable gains, only one hardware design is required with the capabilities of reconfiguring system parameters via these gains. With the model design and selected CMOS devices, we can simulate, test, and debug small and simple power systems. To date we have developed circuit models for generators, lines, and loads [6], [7]. After validation of circuit models and emulator features, the analog emulator can easily move to hardware testing and PCB layout and design.

C. PC Board Development and Emulation

Next is the development of a Printed Circuit Board (PCB) prototype. Presently, each power system component (generator, transmission lines, loads, etc.) is designed on a single PCB. This method requires the power system configuration to be manually connected but allows for easy debugging and computer interaction. This prototype is based on the circuits constructed and simulated in PSpice software. The PCB allows for verification of the circuits and the emulation methodology in analog hardware. Issues such as heat dissipation, energy consumption, data acquisition, system parameter configuration and actuation, noise, and computational accuracy can be analyzed and optimized in analog hardware at this level. National Instruments LabVIEW software is utilized for acquiring data and interfacing with the PCB. The main purpose of this hardware stage is to develop a fully functional small-scale power system emulator in analog hardware.

D. VLSI Board Development and Emulation

In these final steps, we envisage encountering similar issues to those in the previous step of PCB development and emulation. After the debugging process of the analog emulation, the VLSI stage will develop a scaled system on a chip. There are many scalability issues including the following questions:

- Specifically, which power system sizes can be appropriately represented on a given wafer?
- For a given system if more than one chip is required, how will issues of interfacing between these chips be accomplished?

It should also be noted that since we anticipate sizes of up to 5000 or more buses to be emulated, the issues of data acquisition, configuration and actuation have another dimension: communication processing time. Presently, we are conducting feasibility studies of VLSI designs for the PSoC with these issues in mind.

IV. CONFIGURATION, ACTUATION, AND DATA ACQUISITION

In this section, we attempt to detail a scheme to configure, actuate, and acquire data from a large-scale power system emulator. Specifically the process examined is contingency analysis. There are three main steps to the computational process: Initial configuration/reconfiguration of the emulator, emulator actuation/emulation, and data acquisition. The flow chart in Fig. 3 details these steps.

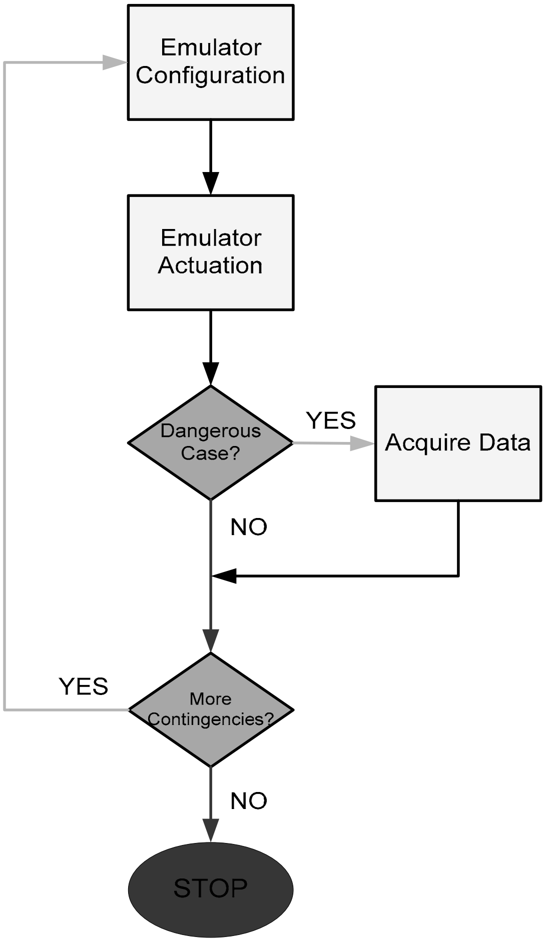

Fig. 3. Emulator Contingency Process

The main steps of the process are detailed by the rectangle boxes. Each of these three processes is detailed below with respect to the analog emulation hardware and the computer interface. Essentially the analog hardware will be doing all the power flow computation and the digital computer will deal with configuring, actuating, and acquiring data from the emulator. Specifically the goal is to minimize the number of pins connecting the host computer to the analog hardware. The main drive for this is practicality. For example with a 40,000-bus power system, measuring bus voltages alone in the analog hardware would require 80,000 measurements (one for real component and one for the imaginary component of each bus). The measurement pins required to interface to a computer are reduced using multiplexing and de-multiplexing strategically. The downside to this is that it creates propagation delays that are tracked and quantified. In addition, the digital-to-analog and analog-to-digital converters also have inherent delay times. The pin count of the interface between the analog emulator and the digital computer is reduced at the cost of overall computation time due to the introduction of additional propagation delays. Overall computation time is defined as the time it takes for the analog computer to solve the problem and data to be extracted.

A. Emulator Configuration

The emulator configuration is conducted via a computer with digital control. This digital control is used to configure all of the analog emulator parameters. This type of configuration only needs to be done once and multiple power flows can be conducted with minimal change in the system. For example, the line parameters once set will not need to be changed every time a power flow case is run. What can change from case to case is the presence of lines for contingencies or generator power output and load power consumption. This process is detailed in Fig. 4.

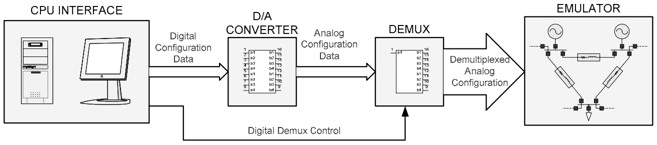

Fig. 4. Emulator Configuration Scheme

It is shown that the digital computer feeds data into a D/A converter, which then goes into a de-multiplexer (DEMUX) to the analog components of the emulator for configuration. For a single D/A converter and DEMUX combination, this is a serial process. The computer provides a single signal to configure a device and the DEMUX is controlled directly by the computer to select which analog device to configure. The DEMUX latches the outputs to maintain the proper configuration as it cycles through the devices. Multiple D/A converters and de-multiplexers can be utilized in parallel to help speed up this process.

B. Emulator Actuation

The next main step is actuating the emulator. This essentially turns the emulator on and off for computation. In Fig. 5, this process is detailed. For the most part the actuation is digital in nature but analog inputs may also be used, which requires the D/A converter. This in itself is quite fast compared to the configuration and data acquisition as there is not as much to do in this stage.

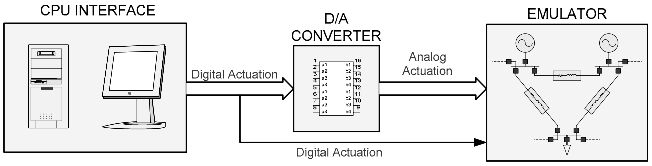

Fig. 5. Emulator Actuation

C. Data Acquisition

The data acquisition scheme is detailed in Fig. 6.

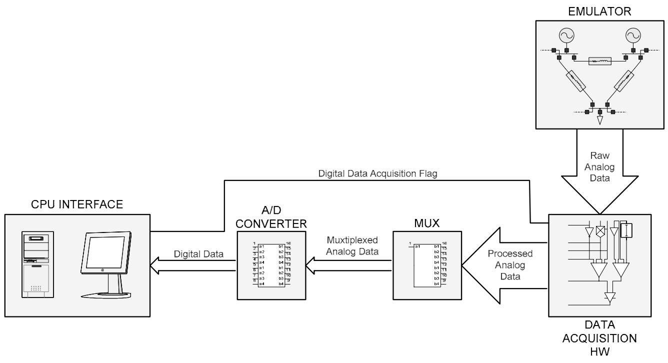

Fig. 6. Emulator Data Acquisition

The analog data acquisition hardware will do two things. First and foremost, it will extract and condition data from the analog emulation hardware for measurement via the digital computer, which is done through A/D converters and Multiplexers. Secondly, it will send a flag to the computer if certain constraints such as voltage magnitude or line current flows are violated during a contingency run. This will tell the digital computer to read back the data for this case. If the flag is not set, the data will not be measured. This helps speed up the contingency computation drastically as data is only extracted for critical contingencies. Again as in the configuration case, the multiplexing and A/D converter is a serial process for one measurement at a time. A parallel combination of converters and multiplexers will speed up this process.

In an initial study, the timings to run an entire n-1 contingency analysis on a sample 40,000 bus power system with the proposed control/actuation scheme (original configuration time not included) can be seen in Table I. The propagation times shown are compiled from individual analog components, which are commercially available.

TABLE I
INITIAL TIMING DATA FOR 40,000 BUS SYSTEM

N-1 Contingency for overall system (excluding setup time)			
Multiplex Channels	**Time for all runs (s)**	**Time to read Data (s)**	**Total Time (s)**
32	0.411264	0.84864	1.259904
64	0.411264	1.69728	2.108544
128	0.411264	3.39456	3.805824
256	0.411264	6.78912	7.200384
512	0.411264	13.57824	13.989504
1024	0.411264	27.15648	27.567744
2048	0.411264	54.31296	54.724224

The higher the number of multiplex channels per multiplexer results in fewer pins required to connect the emulator to the host CPU. Fig. 7, using the results from Table I, shows that as the number of multiplex channels used increases, the total time for one contingency increases. As the number of multiplex channels is increased per multiplexer, the pin count decreases for a single PSoC. Fig. 8 shows the effect of the number of pins of a VLSI device has on the data acquisition time.

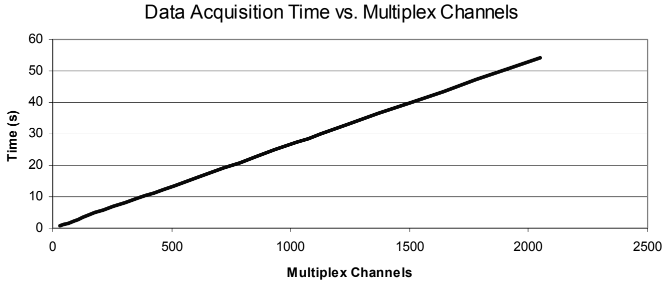

Fig. 7. Timing Effects of Multiplex Channels

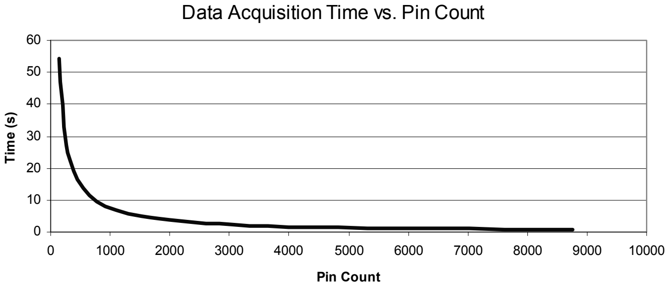

Fig. 8. Timing Effects of Pin Count

Fig. 7 and Fig. 8 represent just some of the issues surrounding the design and fabrication of a VLSI PSoC. Accommodating these issues and others can result in an optimal design of a Power System on a Chip. The next section provides results and discussion for a three-bus power system built using PCB prototype models referred to as modules.

V. RESULTS AND DISCUSSION

The development of this analog power system emulator has consisted of software and hardware components. Power flow cases were conducted in simulation and analog hardware to verify the results from the emulator. Presented in this section are results for ABM based PSpice simulations and hardware results for a three bus power system emulator. The results are compared directly to PowerWorld load flow results. The system consists of two generators (one slack), three lossless transmission lines, and one constant current load. Fig. 9 shows the PowerWorld system with load flow results. These results are compared to the software and hardware results of the analog emulator. Specifically the generator angle and load bus voltages.

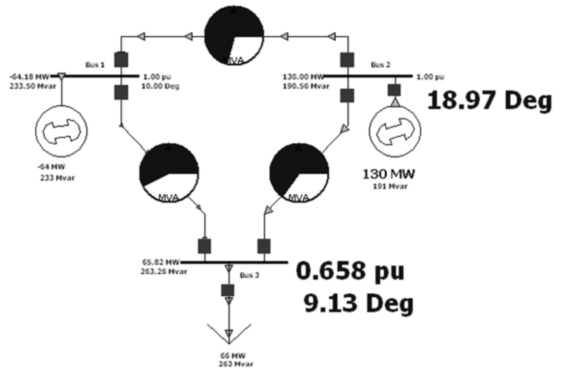

Fig. 9. PowerWorld Results for 3 Bus Power System

PowerWorld only provides the steady-state solution; no dynamics are incorporated into the models. Conversely, the analog emulator includes dynamics in the generator modeling [7], even though our focus in these tests is on steady-state values. The test setup is shown in Fig. 10 for the analog emulator testing. Generator 1 is represented as a slack bus and a second-order model represents Generator 2. The network module consists of the three transmission lines of the system and the load module is a constant current load. The emulator was set up based on the parameters from the PowerWorld case and the system was energized with only the slack bus generator connected. At a specified time generator 2 was switched into the system causing a disturbance. Once the transient settles, the emulator yields the steady-state solution that corresponds to standard load-flow results.

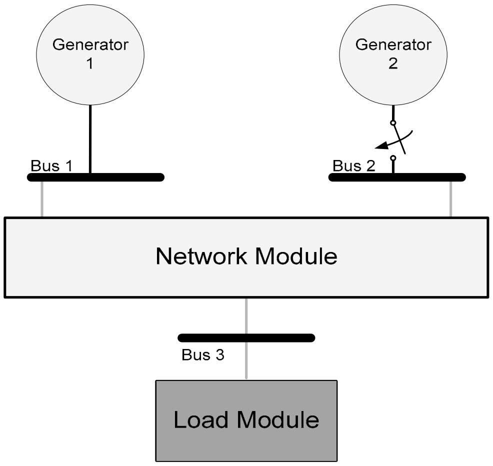

Fig. 10. Three Bus Power System Emulation Setup

A. ABM Emulation Results

In our emulation testing, the voltage was arbitrarily scaled by a factor of two. In other words, one volt per unit in PowerWorld corresponds to two volts in the analog hardware. The ABM simulation results are shown in Fig. 11. The plot shows the generator angle in radians and the real and imaginary load bus voltages. The simulation time is not sped up in this case. The second generator is switched into the system at five seconds and the transient settles to steady-state around 8.5 seconds. These results are later tabulated in Table II.

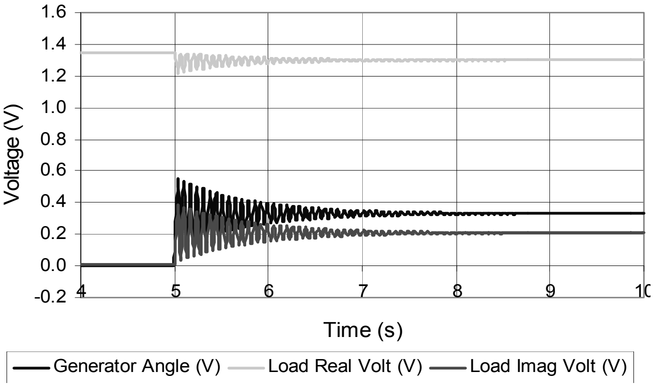

Fig. 11. ABM Emulation Results for Three Bus Power System

B. Hardware Emulation Results

Fig. 12 is a scope capture from the hardware test which monitors the generator angle (top plot), real load bus voltage (middle plot), and the imaginary load bus voltage (bottom plot). The real and imaginary load bus voltages are indicated on the plot as 1.31 and 0.200 volts respectively. Table II shows the results from hardware testing and software simulation of the emulator along with the PowerWorld simulation. The PowerWorld load bus voltages were converted into rectangular coordinates and scaled by a factor of 2 to match the analog emulation.

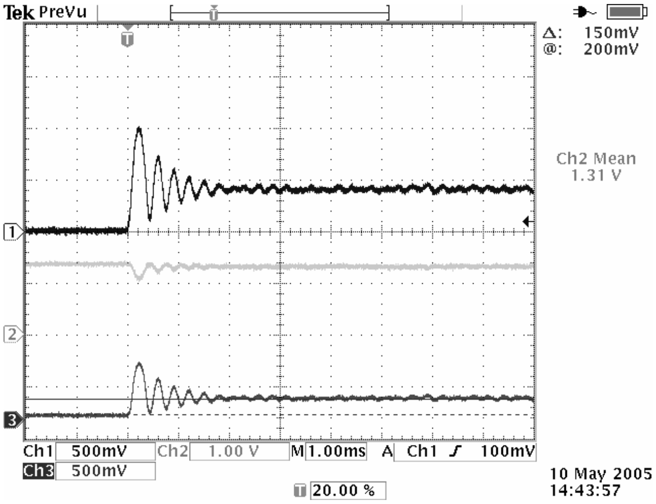

Fig. 12. Hardware Emulation Results for Three-Bus Power System

TABLE II
POWERWORLD AND EMULATOR COMPARISON

		PowerWorld	*ABM Emulation*	*Hardware Emulation*
Generator Angle (deg.)		18.97	18.97	20.40
Load Bus Voltage	Real	1.30	1.30	1.31
	Imaginary	0.21	0.21	0.20

As can be seen the emulation in both software and hardware are very close to the PowerWorld solutions. While the analog computation method lacks precision compared to digital methods the accuracy is quite acceptable. In addition, the hardware emulation was conducted in faster than real time, specifically about 5000 times faster than real time. This can be extremely advantageous in contingency studies when many power flow cases need to be computed in a short period of time. Notably, the speed of analog computation is relatively independent of network size and model complexity. Models that are more accurate can be introduced in analog form without sacrificing computational speed as in digital methods.

VI. CONCLUSION

This paper has exhibited exciting possibilities involved in analog emulation of power systems. The work will lead to the eventual development of a Power System on a Chip (PSoC) that will allow users to obtain analytical results at faster rates that were previously unobtainable. This will offer alternative solutions to growing computational demands such as look-ahead capabilities that lead to enhanced situational awareness of power grids. Future work includes dynamic/transient analysis of power systems as well as VLSI development.

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VIII. BIOGRAPHIES

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