

Analog Emulation of a Reconfigurable Tap Changing Transformer

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Abstract—Accurate analog models of power system components are required in order to realize an analog computation engine for power systems. Analog computation is an area of continued interest and has certain advantages over traditional digital computation. Among the advantages are physically realizable solutions and significantly faster computation times. This paper focuses on the development of a tap changing transformer model designed for a previously proposed method of analog power flow computation. Prior research in this field has modeled generators, loads and transmission lines. The transformer model proposed here provides a more accurate depiction of the network and captures the switching behavior of tap changing transformers. The transformer is modeled in analog form and a controller for the tap changing was developed in digital form. The model is verified via software simulation.

I. INTRODUCTION

Analog computation of power systems is a continuing field of research[1-3]. Among the advantages over traditional digital methods are physically realizable solutions and faster computation times. In order to consummate this analog method as a viable tool in power system analysis accurate models of power system components are required. This paper presents a tap changing transformer model designed for a specific analog computation method.

Currently power flow computation for large power systems is time intensive. The calculations are non-linear in nature and lengthy iteration schemes are the currently preferred solution. This presents a problem as many assumptions and simplifications are required to solve the equations in a timely manner. In addition, the expansion of the power grid, increasing necessity and complexity of contingency studies and introduction of economic analysis are demanding further computational burden. Traditional digital methods are slow to solve the aforementioned demands quickly. This affects the security, reliability and market operation of power systems. Ideally a real-time computation tool is preferable, specifically in market

activities and operation. Analog computation provides a viable alternative to meet this goal.

The main strength of analog computation is speed and parallelism. The power flow solution is obtained almost instantaneously regardless of the number of components in the network. The solution is obtained as quickly as the system stabilizes. Experimentation has shown the ability to calculate solutions even faster than real time. In prior research simulation time for a two machine system were typically 10^4 times shorter than the real time simulated phenomena[4]. This is following the approach of modeling generator dynamics for the purpose of transient stability evaluation. At equilibrium, this dynamic generator model provides steady state solutions to power flow. Prior research has developed static and dynamic generator models [4-6], dynamic load models [7] and static transmission line models [2, 8] for the analog computation scheme utilized here. The work in this paper introduces a transformer model which has the following characteristics:

- Remotely reconfigurable parameters
- Load voltage regulation via tap changing
- Faster than real time computation

The transformer model proposed in this paper enhances the currently existing network model for this computation scheme.

The next section gives an overview on the analog emulation scheme followed by a section presenting the details of the static transformer model. Simulation results in an emulation environment are then shown to verify the functionality of the transformer model.

II. DC EMULATION METHODOLOGY

A DC emulation power flow method has been proposed in [2] and is reviewed here for an understanding of the application for the transformer model in this paper. This approach utilizes multiple resistive networks to compute AC power flow in rectangular coordinates with DC voltages and currents. A figure for a three bus system can be seen in[8].

The emulation is based on the following equation solved in rectangular coordinates:

$$I = Y \cdot V = I_{\text{Re}} + jI_{\text{Im}} = \begin{aligned} & (Y_{\text{Re}}V_{\text{Re}} - Y_{\text{Im}}V_{\text{Im}}) \quad \{\text{real current}\} \\ & + j(Y_{\text{Im}}V_{\text{Re}} + Y_{\text{Re}}V_{\text{Im}}) \quad \{\text{imaginary current}\} \end{aligned} \quad (1)$$

where the subscripts “Re” and “Im” refer to real and imaginary components respectively.

Each of the four current components seen in (1) are represented by a DC voltage dropped across a resistor. This results in four DC resistive networks which represent the AC power system network. The power system in this emulation is broken up into three main components: generators, network and loads. The generators are represented as DC voltage sources, the power system network as resistive networks whose size is relative to the network parameters and the loads sink current from these networks. Note that this network model requires the network to be represented by fixed impedances. System frequency is assumed to be constant. The generators excite the networks with real and imaginary DC voltage components and the states (voltages and currents) of the resistive networks provide the AC power flow solution.

The generator in this analog computation scheme has to supply the appropriate power to the DC networks. The generator was modeled dynamically via the swing equation and maintains a PV behavior[5]. The generator angle is solved for by balancing mechanical power input and electrical power output:

$$M \ddot{\delta} + D \dot{\delta} + P_e(\delta) = P_m \quad (2)$$

With the angular solution of (2), obtained via analog integrators, the appropriate voltages in rectangular coordinates are applied to the emulation networks governed by analog sine and cosine shapers:

$$V_{\text{Re}} = |V| \cdot \cos(\delta) \quad (3)$$

$$V_{\text{Im}} = |V| \cdot \sin(\delta) \quad (4)$$

The load is modeled dynamically as a PQ bus interfacing with the DC emulation networks. Refer to [7] for details. The transformer model is lumped into the power system network and was developed to function in the framework of this DC emulation scheme.

III. ANALOG TRANSFORMER MODEL

The tap changing transformer model was developed by deriving the DC emulation representation of the transformer from a circuit representation of the transformer. The purpose of this is to develop a model for analog computation that can retrieve similar results to those obtained by digital methods. With the model suitable for DC emulation analog circuits were developed to realize the model which allow for parameter reconfiguration and tap changing control. From

this model control schemes were developed to regulate the load voltage of the transformer.

A. Analog Transformer Model

The circuit representation of the tap changing transformer is shown in Figure 1[9]. It consists of an ideal transformer of a turns ratio 1: t and a series impedance. The computation is done in per-unit with a nominal turns ratio of one.

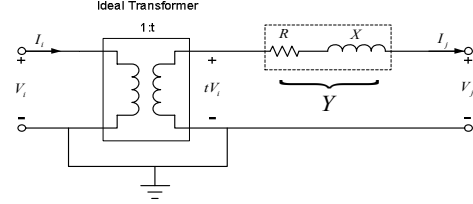


Figure 1. Circuit Representation of Tap Changing Transformer

Developing equations for the voltages and currents in the circuit yields the following equation:

$$\begin{bmatrix} I_i \\ I_j \end{bmatrix} = \begin{bmatrix} |t|^2 Y & -t^* Y \\ -t Y & Y \end{bmatrix} \begin{bmatrix} V_i \\ V_j \end{bmatrix} \quad (5)$$

A pi equivalent circuit can be developed for this transformer from (5) so long as the tap setting t does not have a phase shift. If a phase shift is present the off diagonal entries of (5) become unequal and the circuit will no longer be realizable. This pi equivalent circuit of the transformer is shown in Figure 2. In order to be used in DC emulation this equivalent circuit of the transformer was transformed into rectangular coordinates similar to equation (1) and is represented in emulation with four DC resistive networks.

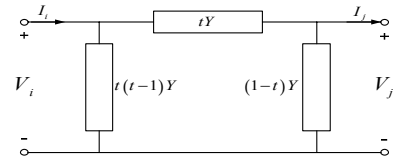


Figure 2. Equivalent Circuit of Tap Changing Transformer

The four DC emulation networks are constructed to emulate the behavior of the tap changing transformer as shown in Figure 3.

The circuit resistors for the DC networks are sized as follows:

$$R_{x(ij)} = \frac{1}{tY_x} \quad (6)$$

$$R_{x(i0)} = \frac{1}{t(t-1)Y_x} \quad (7)$$

$$R_{x(j0)} = \frac{1}{(1-t)Y_x} \quad (8)$$

where the subscript x specifies either the real (Re) or imaginary (Im) resistor and admittance.

The equivalent circuit of the tap changing transformer shown in Figure 2, is reduced to only the series element tY when a transformer on nominal taps values (1:1 ratio or $t = 1$) is considered. Therefore, the 4 DC networks shown in Figure 3 also get reduced to only the resistors sized by (6).

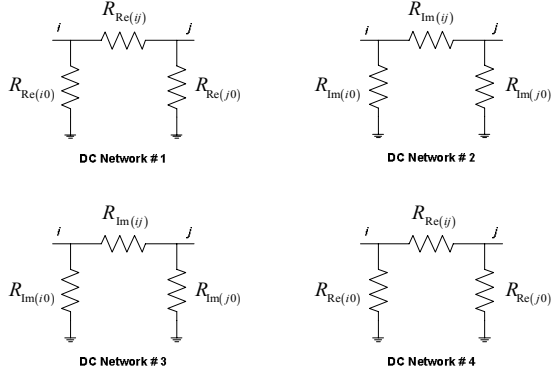


Figure 3. Representation of the Tap Changing Transformer with 4 DC networks

The DC networks can be transferred into circuits using Operational Transconductance Amplifier (OTA) based variable resistors. The OTA based variable resistor shown in Figure 4 [10] consists of two OTAs to address bidirectional current flow. The two inputs (V_1 , V_2) mimic terminals of a resistor and the i_{abc} is the bias current used to control the resistance of the model similar to the wiper on a potentiometer. The effective resistance seen between terminals V_1 and V_2 is governed by the following equation[8]:

$$R_{eff} = \frac{2R + R_A}{g_m R_A} \quad (9)$$

The sizing of resistors R and R_A along with the range of transconductance gain g_m will determine the behavior of the circuit. The transformer is built utilizing these variable resistor circuits in the manner shown in Figure 3. The transformer parameters are remotely controllable and reconfigurable via the bias current in the OTA circuits.

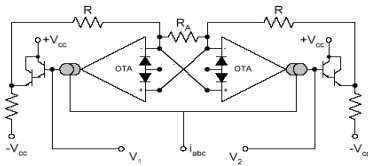


Figure 4. OTA Based Variable Resistor

B. Tap Changer Control

Once the tap changing transformer model is validated, a Printed Circuit Board (PCB) prototype will be built. This PCB will be controlled by LabVIEW which will sense the output voltage of the tap changing transformer. It will next perform logic analysis and calculation of the tap position as shown in Figure 5.

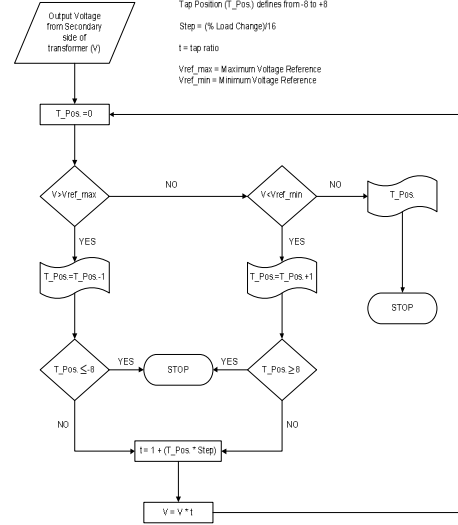


Figure 5. Logic for the digital tap changer control

When emulation is started the tap position is set to zero. The output voltage of the transformer is then sensed and calculations are performed to discretely determine the proper tap ratio in order to regulate the voltage within a specified tolerance. The bias current which is a function of the tap setting, t , is generated from this tap setting and transformer admittance and the OTA variable resistors change accordingly to emulate the behavior of the tap changing transformer. The discrete step of the tap changing transformer is set to 16 steps, eight steps increasing and eight step decreasing. For this logic the voltage references, maximum and minimum reference, and the percentage of load changing are reconfigurable.

IV. SIMULATION RESULTS

Before realizing the actual hardware setup discussed in the previous section, software simulation for the purpose of model validation was performed. Four independent networks containing three LM13700 dual OTA based variable resistors each, were used to simulate a fixed tap, t , tap changing transformer in PSpice. The combination of these networks constitutes the complete test system. The PSpice schematic shown in Figure 6 corresponds to tap changing transformer representation of DC Network # 1. Scaling of system parameters to proper current and voltage level is required to guarantee that the OTA is functioning in the linear operating region.

The value for each OTA based variable resistor is dependent on the tap position t of the transformer. Therefore, OTA based resistors value change to regulate the output voltage of the tap changing transformer. To achieve this, i_{abc} is used to change the value of the OTA based resistor. For the LM13700 the transconductance gain at 25°C is[10]:

$$g_m \approx 19.2I_{abc} \quad (10)$$

Note that for Figure 4, i_{abc} is twice I_{abc} of (10). Taking this into account and using (9) and (10), i_{abc} can be derived as:

$$i_{abc} = \frac{2R + R_A}{9.6R_A R_{eff}} \quad (11)$$

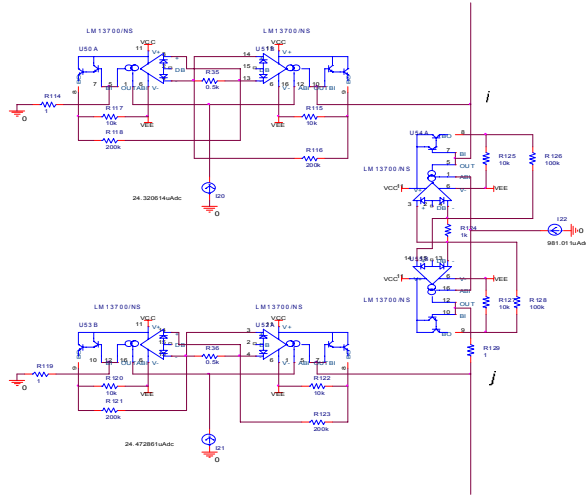


Figure 6. PSPice Schematic of the OTA Based Variable Resistor Tap Changing Transformer

To verify the tap changing transformer model, results from PSPice simulation are compared to those obtained from a traditional load flow solver such as PowerWorld[11]. Currents flowing through the tap changing transformer are compared in Table I.

TABLE I. COMPARISON OF RESULTS

	Amplitude (A)	Difference	Angle (deg)	Difference
PowerWorld	2.047191	-	11.1152	-
Pspice OTA	1.707900	0.339291	22.5695	11.4543
Pspice OTA Offset Correction	2.045712	0.001479	11.8291	0.7139

The analog emulator produces an error if compared with the result from PowerWorld. This error can be attributed to the non-ideal characteristics of the OTA. Refer to [8] for further details. A method for eliminating OTA offset characteristics has been proposed in[12]. This method is suitable for fabrication and quantifies and eliminates the offset for any gain configuration. Here, to compensate for this error, an offset correction method was applied during the post-processing of data. The output current of the OTA based variable resistor circuit is nonzero when no voltage is applied to the input. For post-processing correction, this offset is subtracted from Pspice emulator simulation for the given input voltage. Table I shows the results of the offset correction compared to the original results of the analog emulator. With the offset correction, the amplitude and

angle current is much closer to the desired PowerWorld solution.

V. CONCLUSION

This paper formulates, by means of the equivalent circuit and the proposed DC emulation technique in [2], a model for a tap changing transformer. The analog circuit realization consists of various OTA reconfigurable based variable resistors. Simulation results verify the design of the model and examined the errors introduced by the OTAs. With the offset cancellation of the PSPice solution, the corrected amplitude and angle current closely matches the desired PowerWorld solution.

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REFERENCES

- [1] G. E. R. Cowan, R. C. Melville, Y. P. Tsividis, "A VLSI Analog Computer/Digital Computer Accelerator", *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, 2006
- [2] R. Fried, R. S. Cherkaoui, C. C. Enz, A. Germond, and E. A. Vittoz, "Approaches for analog VLSI simulation of the transient stability of large power networks," *IEEE Transactions on Circuits and Systems I-Fundamental Theory and Applications*, vol. 46, pp. 1249-1263, 1999.
- [3] S. P. Carullo, M. Olaleye, and C. O. Nwankpa, "VLSI Based Analog Power System Emulator for Fast Contingency Analysis," *Proceedings of the Hawaii International Conference on System Science*, pp 1-8, January 2004.
- [4] R. Fried, R. S. Cherkaoui, and C. C. Enz, "Low-Power CMOS, Analog Transient-Stability-Simulator for a Two-Machine Power System," *Proceedings of the International Symposium on Circuits and Systems (ISCAS)*, pp. 137-140, June 1997.
- [5] J. Yakaski, Q. Lui, and C. Nwankpa, "Analog Emulation Using a Reconfigurable Classical Generator Model for Load Flow Analysis," *Proceedings of Power Systems Computation Conference (PSCC)*, 2005.
- [6] A. St.Leger and C. Nwankpa, "Static Generator Model for Analog Power Flow Computation," *Proceedings of International Symposium on Circuits and Systems (ISCAS)*, pp. 1687-1690, 2006.
- [7] A. Deese and C. O. Nwankpa, "Emulation of Power System Load Dynamic Behavior Through Reconfigurable Analog Circuits," *International Symposium on Circuits and Systems (ISCAS)*, pp. 1691-1694, 2006.
- [8] A. St.Leger and C. O. Nwankpa, "Reconfigurable Transmission Line Model for Analog Power Flow Computation," *Proceedings of the 15th Power Systems Computation Conference (PSCC)*, 2005.
- [9] J. J. Grainger and J. William D. Stevenson, *Power System Analysis*: McGraw-Hill, 1994.
- [10] N. Semiconductor, "LM13700 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers," 2000 <http://www.national.com>.
- [11] "PowerWorld Simulator 10.0," PowerWorld Corporation, 2004 <http://www.powerworld.com>.
- [12] R. Wunderlich, J. Oehm, A. Dollberg, and K. Schumacher, "A Linear Operational Transconductance Amplifier with Automatic Offset Cancellation and Transconductance Calibration," presented at The 6th IEEE International Conference on Electronics, Circuits and Systems, University of Patras, Greece, 1999.