

Effect of Size on Analog Circuit Based Emulation of Steady-State Power System Behavior

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Abstract – This paper further examines the use of analog circuit based emulation to study the behavior of multi-bus power systems, specifically the effect of power system size on the hardware design and performance. The goal is to demonstrate that these effects are minimal and analysis of large power systems through emulation methods is not only a viable but favorable alternative to popular simulation methods.

I. INTRODUCTION

The rise of the digital computer over the last half century revolutionized every aspect of mathematics, science, and engineering. However the operation of these engines will always be dependent on a finite clock period and finite quantization error. This is why a reemergence of analog computational engines has been discussed recently [1]. For many applications, especially those which require a large number of iterative calculations, the limitations of digital computation reveal the need for alternative methods [1].

Examples of such applications are software implementations of the highly iterative Newton-Raphson, Gauss, Gauss-Seidel, and ladder iterative methods for steady-state power flow analysis of large systems [9]. This paper further examines an alternative: the use of component based analog computational engines to study the behavior of such power systems. In analog computation, or emulation, analog hardware utilizes input signals for configuration while measurement devices extract node voltages and branch current flows as solutions [2]. With a reconfigurable design the emulation hardware operates in a similar manner to a software algorithm. Similar to a software algorithm:

- the circuit utilizes a set of input signals to yield a set of desired output unique to that configuration.
- the user requires no knowledge of the hardware's internal operation.

It is notable that this internal operation is more intuitive than that of software algorithms utilizing linear algebraic methods [2].

For large power systems, the size of this analog hardware may be of concern. However the use of VLSI (very large scale integration) technology provides many solutions. Research conducted in this area is producing smaller, more efficient, and more accurate analog chips. Utilizing these advances, it may be possible to place an emulated power system with hundreds or thousands of buses on a single silicon chip [1].

In order to demonstrate that power flow analysis of large systems through analog emulation is a viable alternative to digital simulation methods, it must be shown that the hardware design and control, solution accuracy, and computational time do not suffer with increases in the system size. This paper examines the performance of analog emulation hardware and hypothesizes that it is comparable, and in many cases superior, to the performance of digital simulation methods. The body of the paper will discuss the system setup and effects of system size on hardware design and emulation performance.

II. HARDWARE SETUP

A. Emulation of AC Systems with DC Networks

Fig. 1 depicts a generalized form of the hardware setup utilized to yield the emulation results presented in this paper [1]. In this setup, the complex parameters of the AC power system are converted to a rectangular form to facilitate the emulation with DC networks. Four DC networks conduct the four components of the AC line currents, shown in rectangular form in (1) [2].

For a lossless power system, in which line conductance values (G) are negligible, only two DC networks are required to conduct current [2].

$$(1) \quad I = \left(\underbrace{GV_{\text{Re}}}_{I_{\text{NET1}}} - \underbrace{BV_{\text{Im}}}_{-I_{\text{NET2}}} \right) + j \left(\underbrace{BV_{\text{Re}}}_{I_{\text{NET3}}} + \underbrace{GV_{\text{Im}}}_{-I_{\text{NET4}}} \right)$$

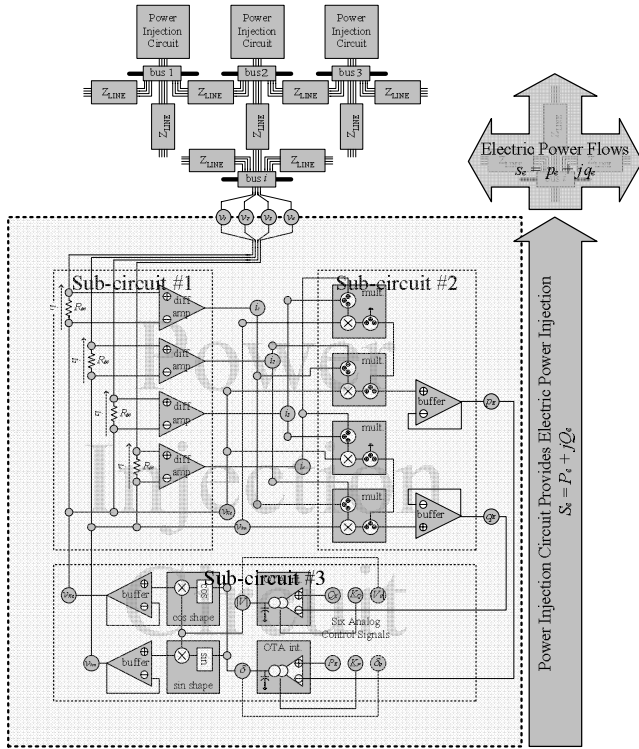


Fig. 1. Emulated Power System Setup with Simplified Power Injection Circuit Schematic

B. Power Injection Circuit

In this setup each bus is generic. A power injection circuit attached to each bus injects (either positive or negative) power into the network. The steady-state behavior of this circuit can be configured to mimic any type of constant power load or voltage controlled bus [6] [9]. With the addition of small sub-circuits generator VAR limits and constant impedance or current load behavior can be incorporated.

Equations (2) and (3) describe the dynamic behavior of the power injection circuit for operation as a constant power load bus [8]. Both the bus voltage magnitude and angle are dependent on a comparison of the corresponding steady-state electric power injections (P_E^* , Q_E^*) and instantaneous (p_E , q_E) electric power flows [4]. For voltage controlled buses, the dynamic behavior of the power injection circuit is described only by (3) as the bus voltage magnitude is maintained constant [8].

$$(2) \quad \frac{\partial |V|}{\partial t} = |K_Q| (Q_E^* - q_E)$$

$$(3) \quad \frac{\partial \delta}{\partial t} = |K_P| (P_E^* - p_E)$$

Common analog components compose the power injection circuit: operational amplifiers, four-quadrant analog multipliers, operational transconductance amplifier (OTA)

based integrators [5], and sine/cosine shaping chips. The circuit utilizes measurements of the bus current flows to update the internal real and imaginary bus voltages (v_{Re} , v_{Im}) as dictated by (2) and (3). This scheme allows for the regulation of the bus electric power flows [6].

Fig. 1 presents a simplified schematic of the power injection circuit's feedback design. The first sub-circuit applies the internal real and imaginary bus voltages, as updated by analog hardware, to the external network bus (v_1 , v_2 , v_3 , v_4). The voltage drop across the small R_M resistor is minimal. It also utilizes a set of differential amplifiers to measure the four DC current flows (i_1 , i_2 , i_3 , i_4) to the network bus. A second sub-circuit utilizes those four measurements in conjunction with the internal real and imaginary bus voltages to calculate the instantaneous electric power flows. A third sub-circuit performs a comparison of the instantaneous power flows and steady-state power injections and, utilizing an OTA based integrator circuit, updates the bus internal voltage magnitude ($|V|$) and angle (δ) [11]. The updated internal bus voltage, in rectangular form, is fed back to the first and second sub-circuits [6].

Six analog input signals dictate the operation of the power injection circuit:

- the steady-state power injections (P_E^* , Q_E^*)
- the integration time constants (K_P , K_Q)
- the bus initial conditions ($|V_0|$, δ_0)

Note that instantaneous power flows are the result of calculations performed by sub-circuit #2. For operation as a voltage controlled bus, the voltage magnitude is not allowed to vary from the initial condition [8].

C. Transmission Line Circuit

In this setup each transmission line is generic. Each connection is modeled as a lumped pi transmission line [7]. For emulation of AC power system with DC networks the complex line impedances are represented as four resistances [2]. The transmission line circuit's design utilizes an OTA based floating voltage controlled resistor to conduct bidirectional line currents [7]. The OTA's amplifier biasing current (i_{ABC}) dictates the circuit's operation. This input may vary the impedance of any transmission line within several orders of magnitude, including an open line condition [5].

III. PERFORMANCE EFFECTS

A. Method of Analysis and Comparison

For the analysis below, two types of results are discussed: emulated and simulated. Emulated results refer to the solutions yielded by simulation of the reconfigurable analog circuits discussed in section 2 by Cadence PSPICE PSD 15.2 [13]. The design utilizes only models of commercially available components. Simulated results, used as a benchmark in most cases, refer to those solutions

yielded by the Newton-Raphson based MATPOWER v.3.0. power flow solver within MATLAB v.7.0.0 [12].

For these trials, the effect of system size is observed at five levels: 3-bus, 6-bus, 9-bus, 14-bus, and 30-bus. Within this paper, these levels will be referred to as the power system standard test set. While IEEE standards define the 14-bus and 30-bus systems, the 3-bus, 6-bus, and 9-bus systems are taken as subsets of the 14-bus case.

One may argue that the test set, spanning one order of magnitude, does not differ greatly in scale. However traditional digital methods are sensitive to these small changes in size. Utilizing the test set we can gain insight in to the effect of system size on the emulation hardware's operation. This paper will introduce larger systems and discuss how the trends observed in the test set may be extended to any n-bus power system.

B. Hardware Design And Control

When considering the design and control of the emulation hardware, importance is placed upon the effect of system size on:

- required number of active analog components (n_A)
- required number of analog control and measurement signals (n_C)
- required circuit design changes

The number of active analog components required to construct the emulation hardware increases as a function of the number of system buses (n_B) and the number of system transmission lines (n_X). Equation (4) describes this relationship mathematically. The number of active components required to construct a single power injection circuit is denoted as α_B , and the number of active components required to construct a single transmission line circuit is denoted as α_X .

$$(4) \quad n_A = \alpha_B n_B + \alpha_X n_X$$

For the standard test sets, the number of transmission lines grows approximately linearly with the number of system buses. This trend continues in to the larger IEEE standard systems. Fig. 2 shows this trend for systems up to a size of 300-bus.

As these systems represent typical power system topologies, the assumption defined in (5) will be made for all n-bus power systems.

$$(5) \quad n_X \approx \beta n_B$$

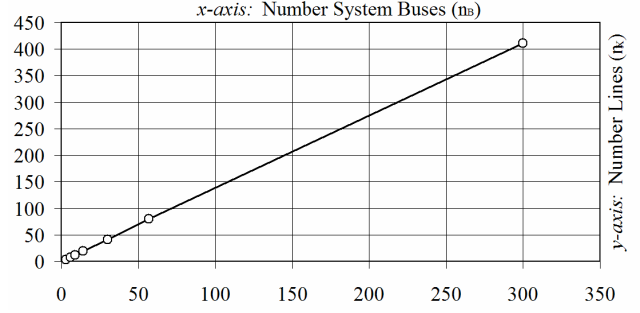


Fig. 2. Number of Transmission Lines vs. System Size for Test Set

Equation (6) shows that, with this assumption, the number of active analog components required to construct the emulation hardware increases approximately linearly as a function of the number of system buses. Though (6) may not yield an exact value for n_A , it does however ensure that a linear function bounds its growth.

$$(6) \quad n_A \approx (\alpha_B + \alpha_X \beta) n_B$$

A relationship similar to that shown in (6) describes the number of analog signals required to control and monitor the emulation hardware. Equation (7) shows that, with the assumption made in (5), the number of analog signals required to control the emulation hardware increases approximately linearly as a function of the number of system buses. The number of analog signals required by a single power injection circuit is denoted as γ_B and the number of analog signals required by a single transmission line circuit is denoted as γ_X . Though (7) may not yield an exact value for n_C , it does however ensure that a linear function bounds its growth [10].

$$(7) \quad n_C \approx (\gamma_B + \gamma_X \beta) n_B$$

The generic design and control scheme of each individual power injection and transmission line circuit is unaffected by changes in system size.

C. Solution Accuracy

When considering the solution accuracy of the emulation hardware at a single bus i , importance is placed upon the effect of system size on the bus voltage solution error (ϵ_i). Equation (8) shows how the solutions, complex voltages at bus i , yielded through emulation (V_i) and simulation (V_i^*) define this value.

$$(8) \quad \epsilon_i \triangleq \left| \frac{\text{Re}(V_i) - \text{Re}(V_i^*)}{\text{Re}(V_i^*)} \right| + \left| \frac{\text{Im}(V_i) - \text{Im}(V_i^*)}{\text{Im}(V_i^*)} \right|$$

We propose the use of the maximum of the individual bus errors to define the voltage solution error for the system (ϵ_S). Refer to (9).

$$(9) \quad \epsilon_S \triangleq \|\epsilon_i\|_{\infty}$$

Fig. 3 shows the relationship between the system voltage solution error and system size for the test set. With the exception of the 3-bus case, the maximum error remains relatively low, less than 1.0%, and does not vary as a function of the number of system buses. The outlier, high maximum error for the 3-bus case, is a result of a light load profile. For this light load profile the simulated voltage solution at the single load bus contains an imaginary component very close to zero. This small value in the denominator of (8) results in a system voltage solution error for the lightly loaded 3-bus case.

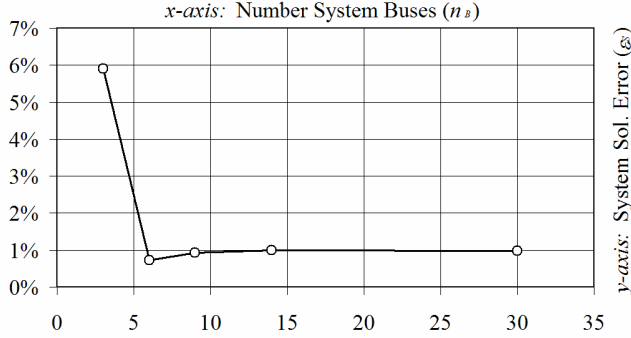


Fig. 3. System Solution Error vs. Power System Size for Test Set

Fig. 4 shows the relationship between the bus voltage solution error (ε) and bus number for the IEEE standard 14-bus power system. As with all the systems in the test set, the distribution of error among the system buses is relatively uniform. The emulated solution does not contain any “weak buses” at which the user should expect an unusually high error. Bus 1 is a statically defined reference.

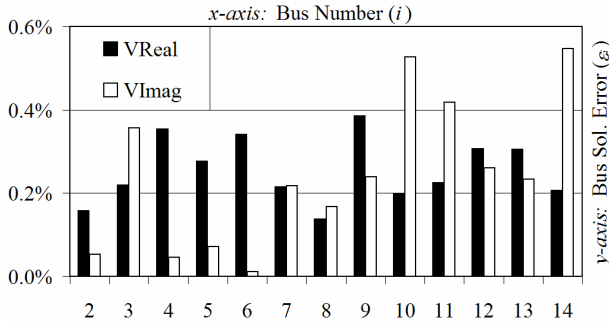


Fig. 4. Bus Solution Error vs. Bus Number for IEEE Standard 14-bus Power System

D. Computational Speed

Equations (10) and (11) define the individual bus settling time (t_i): the length of time required for the step changes of the real and imaginary voltage waveforms at a bus i to fall below a given threshold (ϕ) [11]. When considering the computational speed of the emulation hardware, this value is of importance. It is only when these transients have subsided that bus voltage solutions may be reliably extracted.

$$(10) \quad \Delta v_i(t) = v_i(t) - v_i(t - \delta)$$

$$(11) \quad t_i \triangleq \min\{t : (\text{Re}(\Delta v_i(t)) + \text{Im}(\Delta v_i(t))) < \phi\}$$

We propose the use of the maximum of the individual bus settling times to define the settling time for the system. Refer to (12).

$$(12) \quad t_s \triangleq \|t_i\|_\infty$$

Fig. 5 shows the relationship between the system settling time and system size for the analog emulation hardware in per unit. The base for those per unit values is 1.91 ms: the settling time for the 3-bus system. Fig. 5 also shows the relationship between the computational time and system size for the MATPOWER software in per unit. The base for those per unit values is 9.17 ms: the computational time for the 3-bus system. Equation (13) gives the most fundamental definition of this value: the delay between realization of a solution and utilization of input.

$$(13) \quad t_C = t_{Sol'n} - t_{Input}$$

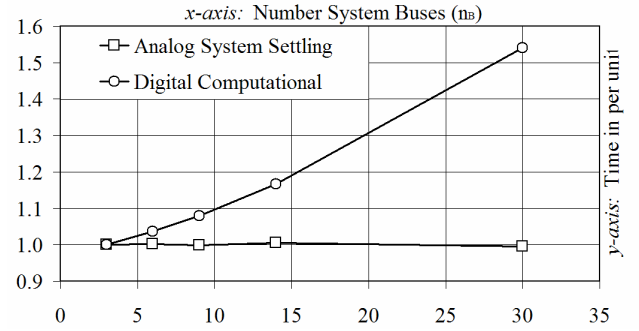


Fig. 5. Analog Settling Time and Digital Computational Time vs. Number of System Buses (n_b) for Test Set

The system settling time for the analog hardware does not vary as a function of the number of system buses. This settling time can be controlled in absolute terms, however, by resizing the capacitors within the OTA based integrator circuits (see fig. 1) or through manipulation of the K_Q or K_P analog input signals (again see fig. 1). Computational time for the digital method varies exponentially as a function of the number of system buses. This observation is supported by that of previous studies [6]. This trend is a sharp contrast to that of the analog system settling time and it highlights one of the main advantages of analog computation: speed.

For any n -bus emulated power network, configuration of and data acquisition from the analog emulation hardware cannot be practically implemented through the utilization of individual analog signals. The time required for digital multi-channel multiplexing devices and digital-to-analog or analog-to-digital converters to perform configuration of and data acquisition from the emulation hardware, not system settling time, will limit solution computational time. Previous studies have shown that these values vary linearly with the system size [10].

TABLE I. CONFIG. / DATA ACQUISITION TIME VS. NUMBER SYSTEM BUSES

Number Buses	System Settling Time (ms)	Config./Data Acq. Time (ms)
40,000	1.910	16.758
27,035	1.910	11.766
7,917	1.910	4.790
1,648	1.910	2.526

IV. CONCLUSIONS

A. Innovation

This paper further examines the use of analog circuit based emulation to study the behavior of multi-bus power systems. The effect of system size on power system emulation has been touched on in the past. However past studies presented results for very small systems or systems emulated with ideal components. Section III, above, presents physically reproducible results for systems emulated with real, commercially available, component models ranging one order of magnitude in size.

This paper also examines the use of complementary metal oxide semiconductor (CMOS) devices, developed for high frequency operation, for emulation. Section II, above, gives insight as to how these devices may be enhanced for low-frequency purposes.

Finally, this paper introduces the utilization of a more generic power system emulator hardware design in which no distinctions between load and generator buses exist. This scheme is beneficial when considering large systems as it significantly reduces the number of analog circuits required for emulation.

B. Performance Conclusions

This paper demonstrates that the use of analog emulation methods is a viable alternative to digital computation, or simulation, for steady-state power flow of large systems.

Section III, above, shows that both the size of the emulation hardware and computational speed vary linearly as a function of the system size. The effect of system size on emulation hardware accuracy is minimal. These individual trends, discussed in parts B, C, and D of Section III, do not only describe performance within the test set. They may be extended to describe the performance of the emulation hardware for power systems of any size.

This conclusion demonstrates that the performance of emulation hardware does not significantly suffer with increases in system size. With respect to design, error, and speed it is comparable, and in many cases superior, to the performance of digital simulation methods. This is most evident with respect to computational speed. This paper shows that the solution computational time for the emulation hardware varies linearly with the system size. This is a great advantage over the exponential relationship between the

solution computational time and system size for digital methods.

The performance of this analog emulation will only improve with advances in CMOS and VLSI technologies [10]. In the future it will provide many promising new opportunities in the field of computation, especially for complex non-linear problems [1].

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REFERENCES

- [1] S.P. Carullo, M. Olaleye, and C.O. Nwankpa, "VLSI Based Analog Power System Emulator for Fast Contingency Analysis", Proceedings of the 37th Hawaii International Conference on System Sciences, p. 60-67, January 2004.
- [2] R. Fried, R.S. Cherkaoui, C.C. Enz, A. Germond, and E.A. Vittoz, "Approaches for Analog VLSI Simulation of the Transient Stability of Large Power Networks", IEEE Transactions on Circuits and Systems - I, Vol. 46, No. 10, p. 1249-1263, October 1999.
- [3] W. H. Kersting, "Distribution System Modeling and Analysis", CRC Press: London, 2002, ISBN 0-8493-0812-7, pp 251 – 266.
- [4] C.O. Nwankpa, S.M. Shahidehpour, and Z. Schuss, "A Stochastic Approach to Small Disturbance Stability Analysis", IEEE Proceedings of Power Systems, Vol. 7, Issue 4, p. 1519 – 1528, November 1992.
- [5] R. L. Geiger and E. Sánchez-Sinencio, "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," IEEE Circuits and Devices Magazine, Vol. 1, p. 20 – 32, March 1985.
- [6] M. Olaleye and C. O. Nwankpa, "Analog Behavioral Models for the Purpose of Analog Emulation of Large Scale Power Systems, " The Proceedings of the 36th North American Power Symposium (NAPS), p. 97 – 104, August 2004.
- [7] A. St. Leger and C. Nwankpa, "Reconfigurable Transmission Line Model for Analog Power Flow Analysis", Proceedings of 2005 Power Systems Computation Conference, Liege, Belgium, August 2005
- [8] J. Yakaski, Q. Liu and C. Nwankpa, "Analog Emulation using Reconfigurable Classical Generator Model for Load Flow Analysis", Proceedings of 2005 Power Systems Computation Conference, Liege, Belgium, August 2005.
- [9] J. J. Grainger and W.D. Stevenson, "Power System Analysis", McGraw Hill Publishing, 1994, ISBN 0-07-061293-5, p. 332 – 333
- [10] C.O. Nwankpa, A. Deese, Q. Liu, A. St. Leger, J. Yakaski and N. Yok, "Power System on a Chip (PSoC): Analog Emulation for Power System Applications", Accepted for Publication within Proceedings of 2006 Power Engineering Society General Meeting, Montreal, Canada, June 2006.
- [11] A. Deese and C.O. Nwankpa, "Emulation of Power System Load Dynamic Behavior Through Reconfigurable Analog Circuits", Accepted for Publication within Proceedings of 2006 International Symposium on Circuits and Systems (ISCAS), Kos Island, Greece, May 2006.
- [12] Etter, D.M. "Engineering Problem Solving using MATLAB Prentice Hall, 1993.
- [13] Rashid, M.H. "Spice for Circuits and Electronics using PSPICE Prentice Hall, Second Edition, 1995.