Configuration of a Large Scale Analog Emulator for Power System Analysis

Aaron St. Leger, *Student Member, IEEE,* and Chika O. Nwankpa, *Member, IEEE*

Abstract— **This paper provides a systematic approach to configure a large scale analog emulator for power system analysis. Historically this involved magnitude and time scaling of parameters and consisted of many trials and errors. A recently developed remotely reconfigurable analog power system emulator contains operational transconductance amplifiers and thus has limited linear operating ranges. Scaling of the power system parameters is critical to ensure accurate results and keep the analog hardware operating in linear regions. The configuration method proposed here determines analog hardware gains along with magnitude and time scaling parameters to ensure the analog hardware properly emulates the power system in a systematic manner which could be automated via software and remote control of the hardware. An example is provided for a single machine infinite bus system.**

Index Terms— **Analog Computers, Computation Theory, Power System Simulation, Programming**

I. Introduction

Analog computation of power systems has many advantages over digital computation. Traditional digital methods are expensive and slow in comparison to analog computers. With analog methods the solution time is independent of system size. One of the weaknesses of this analog approach is the configuration, or programming, of the system. Historically configuring large scale analog computers has been very time consuming. The analog computer parameters must be scaled and configured (historically manually) in relation to the real world system it is representing. Most literature on the subject [1-4] separates the scaling into two main components: time and magnitude.

Time scaling allows analog computers to calculate in real time and faster or slower than real time. Magnitude scaling is defined as "the process through which a linear relationship is established between the voltage at any reference node and the variable represented by it"[5]. The scaling process traditionally involved a trial and error approach. "Rough estimation of maximum values and fine tuning gains for small/large values"[4] until the analog computer is within operating regions (i.e. no overloads) and acceptable noise levels for measurement. In the past "a large simulator is often setup in a number of stages"[4]. The approach in this paper systematically configures a large scale analog power system emulator.

Manuscript received April 21, 2007. This work was supported by the U.S. Department of Energy under Grant No. CH11171.

C. O. Nwankpa is with the Electrical and Computer Engineering Department, Drexel University, Philadelphia, PA 19104 USA (phone: 215-895-1466, fax:215-895-1561, e-mail: nwankpa@ece.drexel.edu

II. Problem Formulation

In analog computation the limitations of the hardware, namely linearity and stress, must be addressed. The hardware must be configured to allow proper emulation of the system without violating the constraints of the circuitry. In addition, signal fidelity must be maintained to ensure measurability of the solutions, which are analog voltages and currents.

The power system model being employed here consists of interconnected generators, transmission lines and loads. The analog computation method of DC emulation [6] and reconfigurable analog hardware for the generators [7] transmission lines [8] and loads [9] have been developed. Within this framework the proposed configuration method was developed.

Historically the components of analog computers (resistors, op-amps, etc.) are highly linear in a large operating range, specifically, levels of 10 or 100V. In the DC emulation hardware the levels are much lower due to nonlinear devices. For example, the linear operating range of a BJT based operational transconductance amplifier (OTA) is ±25mV [7] and ±1mA [10]. Due to the heavy implementation of OTAs this power system emulator is highly non-linear.

An application of this emulator is transient stability analysis. With trial and error methods, it is not possible to ensure operation within linear regions. The approach taken here is to ensure all stable cases fall within linear regions. If this is accomplished saturation may be used as an indicator for instability. The following are goals set for the configuration of the analog emulator to ensure proper operation:

- Scale the power system parameters and states within analog hardware limits/linear ranges.
- Stable cases should not result in saturation
- Maintain adequate signal fidelity of measured signals.

The following section of this paper describes the technique of power system emulation used and the associated mathematical and analog circuit models. It also derives the limitations of the power system and the analog hardware. The next section details emulator configuration. Then an example is provided followed by a conclusion.

III. Power System Analog Emulation

This section presents the mathematical models of the power system components and analogous circuit models based on the emulation hardware. All of the power system parameters and device limits are defined as well as the gains and limitation of the analog hardware. With this information the hardware is configured to properly represent the power system.

A. Power System Models

The power system model consists of 2nd order generators, static transmission lines and 1st order exponential recovery load models. The generators are based on the swing equation:

$$M\ddot{\delta} + D\dot{\delta} + P_E(\delta) = P_M \quad (1)$$

where M is the generator inertia coefficient, D is the damping coefficient, P_e is the electrical power output and P_m is the mechanical input power. With damping neglected (D = 0) this equation is shown in block diagram form in Fig. 1.

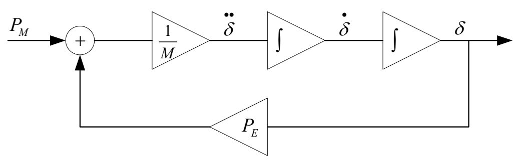

Fig. 1: Block Diagram of Generator Model

The transmission lines are modeled as lossy lines with a series resistance and inductance. The load is modeled as a decoupled PQ dynamic load as presented in [9, 11, 12]. The real and reactive power injections are dependant on the load voltage angle and magnitude as follows:

$$\begin{aligned} P_L + K_P\dot{\theta} &= -P_e(\delta) \\ Q_L + K_Q\dot{V} &= -Q_e(\delta) \end{aligned} \quad (2)$$

where P_L and Q_L are the specified real and reactive power of the load respectively, K_P and K_Q are the time constants associated with the real and reactive power respectively, and P_e and Q_e are the electrical real and reactive power injected into the network. This equation is shown in block diagram form in Fig. 2:

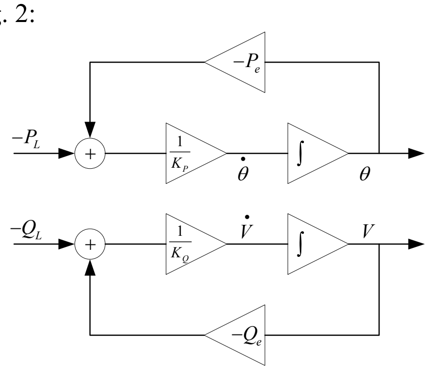

Fig. 2: Block Diagram of PQ Load Model

B. Power System Operation

The power system operating ranges are defined as intervals and detailed in Tables I, II. States of the system are labeled in bold. These intervals identify the operational limitations of the real world power system to be emulated in analog hardware. For example, an interval V_G for generator terminal voltage is defined as:

$$[V_G] = [\underline{V_G}, \overline{V_G}] := \{\widetilde{V}_G \in \mathbb{R} \mid \underline{V_G} \le \widetilde{V}_G \le \overline{V_G}\} \quad (3)$$

where $\underline{V_G}$ is the infimum and $\overline{V_G}$ is the supremum of the generator terminal voltage $\widetilde{V}_G$. The entries in the tables are all vectors with the exception of line impedance interval. For example, if there are *m* generators then δ_G is an *m* dimensional vector of intervals for all *m* generators.

The intervals related to power system parameters such as mechanical input (P_M) and terminal voltage (V_G) of generators, line current limits (I_T) and impedance values (R_T and X_T) and load power (P_L and Q_L) can be obtained from system data. Determining the intervals related to the system states requires more analysis. Our proposed approach considers practical stability limitations of the system and utilizes linear approximations of transient system behavior. The system is linearized around an operating point and trajectories of states are estimated for a given perturbation. Intervals for the states are determined from these estimated trajectories.

TABLE I
POWER SYSTEM NETWORK OPERATING RANGES

Component	Parameter	Interval
Generator	**Terminal Voltage**	$[V_G]$
Transmission Lines	Current	$[I_T]$
	Resistance	$[R_T]$
	Reactance	$[X_T]$
Loads	**Voltage**	$[V_L]$

TABLE II
POWER SYSTEM DYNAMIC OPERATING RANGES

Component	Parameter	Interval
Generator	Input Power	$[P_M]$
	Angle	$[\delta_G]$
	Angular Velocity	$[\dot{\delta}_G]$
	Angular Acceleration	$[\ddot{\delta}_G]$
Loads	Real Power	$[P_L]$
	Reactive Power	$[Q_L]$
	Voltage	$[V_L]$
	$\frac{dV}{dt}$	$[\dot{V}_L]$
	Angle	$[\theta_L]$
	Angular Velocity	$[\dot{\theta}_L]$

For stable operation of generators the limitations on the angle are restricted to ±π/2. To find the interval of the generator angular velocity and angular acceleration the swing equation is linearized about an operating point:

$$M_i\Delta\ddot{\delta}_i + \Delta P_{Ei} = \Delta P_{Mi} \quad (4)$$

For a given perturbation the linearized swing equation can be solved for $\Delta\delta_i(t)$. The final quasi-steady state expression for the generator angle is then:

$$\delta_i(t) = \Delta\delta_i(t) + \delta_i^0 \tag{5}$$

where δ_i^0 is the initial angle of generator i before the perturbation. This is an approximation of the generator response to a disturbance. The response of the angular velocity and acceleration can also be obtained from this. From these waveforms the associated intervals for a given disturbance are quantified. For example, if equation (4) is homogeneous, $(\Delta P_{Mi} = 0)$, $\Delta\delta_i(t)$ will be a sinusoidal function and $\delta_i(t)$ will be a sinusoidal function with an offset as shown in Fig. 3. By taking the first and second derivatives of equation (5) with respect to time the expressions for angular velocity and acceleration are obtained:

$$\begin{aligned} \dot{\delta}_i(t) &= \Delta\dot{\delta}_i(t) \\ \ddot{\delta}_i(t) &= \Delta\ddot{\delta}_i(t) \end{aligned} \tag{6}$$

which are zero mean sinusoidal functions. For this case the infimum and supremum values of angular velocity and acceleration for a given generator i are:

$$\begin{aligned} \overline{\dot{\delta}_{Gi}} &= \overline{\ddot{\delta}_{Gi}} = \overline{\delta_i} - \delta_i^0 \\ \underline{\dot{\delta}_{Gi}} &= \underline{\ddot{\delta}_{Gi}} = \underline{\delta_i} - \delta_i^0 \end{aligned} \tag{7}$$

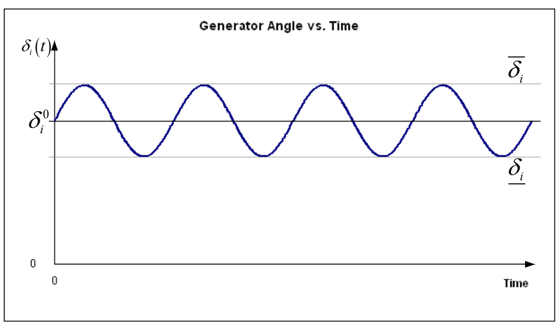

Fig. 3: Generator Angle vs. Time

A similar process can be utilized on the load model to quantify the intervals listed in Table II. To find the operating ranges of load voltage magnitude and rate of change along with the load angle and angular velocity equation (2) is linearized around an operating point. For a load at bus i:

$$\begin{aligned} \Delta P_{Li} + K_{Pi}\Delta\dot{\theta}_i &= \Delta P_{ei} \\ \Delta Q_{Li} + K_{Qi}\Delta\dot{V}_i &= \Delta Q_{ei} \end{aligned} \tag{8}$$

For a given perturbation these linearized equations can be solved. The quasi-steady state expressions for the load voltage magnitude and angle are:

$$\begin{aligned} |V_i|(t) &= \Delta|V_i|(t) + |V_i^0| \\ \theta_i(t) &= \Delta\theta_i(t) + \theta_i^0 \end{aligned} \tag{9}$$

where $|V_i^0|$ and θ_i^0 are the initial load voltage magnitude and phase respectively.

For a stable case both the voltage and phase angle will be exponential curves settling to a steady state value. Fig. 4 shows the response of the load voltage magnitude for a given disturbance. From this waveform the interval of the load voltage magnitude can be obtained. Similarly the interval for the load voltage angle can be obtained. By taking the first derivatives of equation (9) expressions for the rate of change of load voltage magnitude and angular velocity are obtained:

$$\begin{aligned} \dot{|V_i|}(t) &= \Delta\dot{|V_i|}(t) \\ \dot{\theta}_i(t) &= \Delta\dot{\theta}_i(t) \end{aligned} \tag{10}$$

which for stable cases are functions which exponentially decay to zero. The intervals for a given load are determined by examining infimum and supremum of equations (9) and (10). This is conducted for all generators and loads of the system.

Methods to obtain all of the power system intervals detailed in Tables I, II for a single disturbance have been presented. A collection of disturbances and initial conditions could be used to find the intervals for a wide range of cases. All the intervals in Table I are enumerated in a vector $\mathbf{PS_N}$ of intervals and Table II in a vector $\mathbf{PS_D}$. The next section analyzes the operating ranges of the analog circuitry used in emulation.

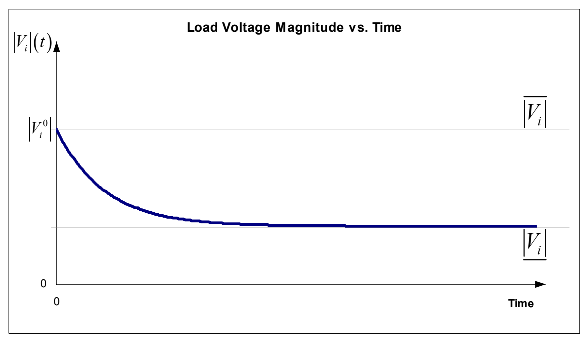

Fig. 4: Load Voltage Magnitude vs. Time

C. *Analog Hardware Models*

The analog hardware models were developed based upon the DC emulation scheme and the models in the prior section. The DC emulation approach models the AC power system network in rectangular coordinates. The result is four DC resistive networks modeling an AC power system network. Refer to [6] for details. These networks are constructed in hardware via nonlinear OTA based variable resistive circuits [8].

The generators and loads are modeled as power injections into the DC resistive networks. A block diagram of the generator analog hardware is shown in Fig. 5. It is analogous to the generator model in Fig. 1 and consists of many amplifiers and integrators. In the notation V and I represent voltage and current respectively while the subscript indicates which parameter is being represented by a given current or voltage (e.g. V_{Pm} is the mechanical input to the generator (Pm) represented by a voltage). The gains which can be scaled and set in hardware are indicated by K_i. Table III enumerates the different gains, their physical units and their function.

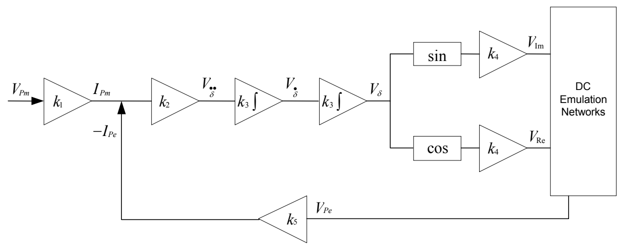

Fig. 5: Block Diagram of Analog Generator Model

TABLE III
ANALOG GENERATOR GAINS

Gain	Units	Details
k_1	uA/V	Converts V_{Pm} to a current
k_2	mV/uA	Inertia Coefficient/Integrator Gain
k_3	V/V	Inertia Coefficient/Integrator Gain
k_4	V/V	Generator Voltage Magnitude
k_5	uA/V	P_e Feedback

A block diagram of the load analog hardware is shown in Fig. 6 and Table IV lists the gains of the circuit. Some of the analog hardware components have extremely limited operating ranges and nonlinearities, specifically the OTAs. The circuits are designed to operate unsaturated in the linear regions. The overall performance and stable operating region of the circuits is sensitive to the selection of these gains.

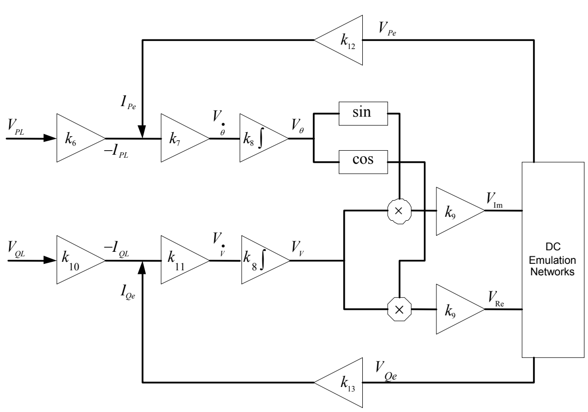

Fig. 6: Block Diagram of Analog Load Model

TABLE IV
ANALOG LOAD GAINS

Gain	Units	Details
k_6	uA/V	Converts V_{PL} to a current
k_7	mV/uA	Time Constant/Integrator Gain
k_8	V/V	Time Constant/Integrator Gain
k_9	V/V	Amplify Voltage to Network
k_{10}	uA/V	Converts V_{QL} to a current
k_{11}	mV/uA	Time Constant/Integrator Gain
k_{12}	uA/V	P_L feedback
k_{13}	uA/V	Q_L feedback

D. Analog Hardware Operation

This section examines the operational ranges of the analog hardware. The analog hardware operation ranges are expressed by intervals listed in Tables V, VI. They are specified in an analogous fashion as the power system operating ranges. The states of the generators and loads are voltages and labeled as in the previous diagrams. The values corresponding to the transmission lines, power injections, and generator terminal voltages are labeled as they were for the power system but with lowercase subscripts. For example the interval for power system generator voltage is V_G while the analog hardware generator voltage interval is V_g.

By the nature of the analog hardware there is a decoupling between the integrators for the generators/loads and the power injection into the emulation networks. The amplifiers with gains k_4 and k_9 provide the voltage and power to the networks. V_g and V_V are related to V_δ and V_l by:

$$\begin{aligned} \left[V_g\right] &= k_4\left[V_\delta\right] \\ \left[V_l\right] &= k_9\left[V_V\right] \end{aligned} \tag{11}$$

The transmission lines are emulated in hardware via OTA based variable resistors. The resistance of the circuit is a function of the OTA bias current i_{abc} which has a finite operating range (e.g. 0 to 1mA). R_t and X_t are found by evaluating the resistance of the circuit at the maximum and minimum bias current values. The I-V characteristic of the circuit is plotted in Fig. 7 for a given resistance. It is clearly seen that the device is highly nonlinear but within a small operating range around 0V input, which is shown on the graph, it is fairly linear. It has been shown in [8] that the saturation is due to the current flow through the circuit. I_t is determined based on the definition of the linear region. The linear region is defined based on a level of acceptable variation seen in the resistance of the circuit. Due to the symmetry of the circuit:

$$\overline{I_t} = -\underline{I_t} \tag{12}$$

A similar nonlinear behavior is exhibited in the analog circuits for the generator [7] and load [9] due to the use of OTA integrators. The other active circuits utilized (op-amps, multipliers, etc.) are fairly linear within the supply voltages. For the purpose of scaling, these circuits are assumed linear and the nonlinear effects are solely due to the OTAs.

The intervals for the generator and load circuits are determined based on the properties of the analog hardware (e.g. voltage source and OTA characteristics). The intervals in Tables V, VI can be enumerated in vectors $\mathbf{HW_N}$ and $\mathbf{HW_D}$ respectively.

TABLE V
ANALOG HARDWARE NETWORK OPERATING RANGES

Component	Parameter	Interval
Generator	**Terminal Voltage**	$[V_g]$
Transmission Lines	Current	$[I_t]$
	Resistance	$[R_t]$
	Reactance	$[X_t]$
Loads	**Voltage**	$[V_l]$

TABLE VI
ANALOG HARDWARE DYNAMIC OPERATING RANGES

Component	Parameter	Interval
Generator	Input Power	$[V_{Pm}]$
	Angle	$[V_{\delta}]$
	Angular Velocity	$[V_{\dot{\delta}}]$
	Angular Acceleration	$[V_{\ddot{\delta}}]$
Loads	Real Power	$[V_{Pl}]$
	Reactive Power	$[V_{Ql}]$
	Voltage	$[V_{V}]$
	$\frac{dV}{dt}$	$[V_{\dot{V}}]$
	Angle	$[V_{\theta}]$
	Angular Velocity	$[V_{\dot{\theta}}]$

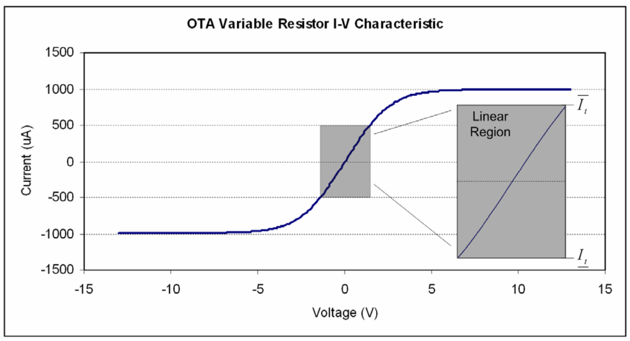

Fig. 7: OTA Variable Resistor I-V Characteristic

IV. EMULATOR CONFIGURATION

This section directly relates the gains and operating region of the analog hardware to the power system parameters and limitations. From this information the power system can be sufficiently scaled in both in magnitude and time for analog emulation. There are equality constraints developed based on time and magnitude scaling of the system along with inequality constraints based on the operating limitations of the system and analog hardware. The scaling is broken into two distinct sections: Scaling of network (voltages, currents, etc.) and scaling of the integrators (magnitude/time scaling).

To scale the integrators the equations for the power system models are written with time (τ) and magnitude scaling (m, k_P, k_Q) factors and compared to the equations for the analog hardware with gains.

$$\delta_{Gi} = m_i \frac{\tau^2}{M_i} \int\int \left(P_{Mi} - P_{Ei}\left(\delta_{Gi}\right)\right) dtdt \quad (13)$$

$$\theta_i = k_{Pi} \frac{\tau}{K_{Pi}} \int -\left(P_{ei}\left(\delta\right) + P_{Li}\right) dt$$
$$V_i = k_{Qi} \frac{\tau}{K_{Qi}} \int -\left(Q_{ei}\left(\delta\right) + Q_{Li}\right) dt \quad (14)$$

The analogous equations for the analog hardware including gain parameters are:

$$V_{\delta i} = k_{2i} k_{3i}^2 k_{1i}^2 \int\int \left(V_{Pmi} - \alpha \cdot V_{Pei}\right) dtdt \quad (15)$$

$$V_{\theta i} = k_{7i} k_{8i} k_{6i} \int \left(\beta \cdot V_{Pei} + V_{PLi}\right) dt$$
$$V_{Vi} = k_{11i} k_{8i} k_{10i} \int \left(\beta \cdot V_{Qei} + V_{QLi}\right) dt \quad (16)$$

where α and β relate the measured power injections into the network and the specified power injections in the integrators for the generator and load respectively and $k_5 = \alpha k_1$, $k_{12} = \beta k_6$ and $k_{13} = \beta k_{10}$.

Relationships between the scaled power system equations and the analog hardware result in the following equality constraints for generators and loads:

$$m_i \frac{\tau^2}{M_i} = k_{2i} k_{3i}^2 k_{1i}^2 \quad (17)$$

$$k_{Pi} \frac{\tau}{K_{Pi}} = k_{7i} k_{8i} k_{6i}$$
$$k_{Qi} \frac{\tau}{K_{Qi}} = k_{11i} k_{8i} k_{10i} \quad (18)$$

The scaling of the network assumes that per unit normalization has already been conducted on the power system. At this point the per unit power system values are scaled to accommodate the analog hardware. This can be accomplished by selecting two scaling values:

$$k_I I = i$$
$$k_V V = v \quad (19)$$

where I and V are the per unit current and voltage respectively, i and v are the analog hardware current and voltage respectively, k_I and k_V are the current and voltage scaling factors respectively.

The scaling factors m, k_P, k_Q, τ, k_I and k_V scale the power system in both magnitude and time for use in the analog hardware. These values and the analog gains k_i are chosen such that the equality constraints in equations (11), (17-19) hold and the following constraints hold:

$$K_N \cdot PS_N \subseteq HW_N$$
$$K_D \cdot PS_D \subseteq HW_D \quad (20)$$

where K_N and K_D are row vectors of the gains relating the power system intervals to the analog hardware intervals. In addition, the gain values for all k_i are restricted by limitations of the analog hardware and signal-to-noise ratios must be higher than a threshold to ensure accurate measurements:

$$k \subseteq K$$
$$M_{sn_i} \geq K_{sn_i} \quad (21)$$

where k is the vector of gains in hardware, K a vector of intervals detailing the ranges of the gains, M_{sn_i} the signal-to-noise ratios for measurement *i*, and K_{sn_i} the minimum signal-to-noise ratios for measurement *i*.

From these constraints the appropriate scaling can be obtained for the emulator. This can be optimized for various objectives such as power consumption, signal to noise ratio, etc. For an example this scaling process was performed on a small system.

V. RESULTS

The proposed configuration procedure was conducted on a singe machine connected to an infinite bus via a lossless transmission line as shown in Fig. 8. The intervals of Tables I, II were obtained from system data and a perturbation of $\left(\Delta\theta_i - \Delta\theta_k\right) = 5^\circ$ and initial conditions of $\delta_1 = 14.478^\circ$, $\dot{\delta}_1 = \ddot{\delta}_1 = 0$. The intervals for the analog hardware obtained from test data are enumerated in Table VII.

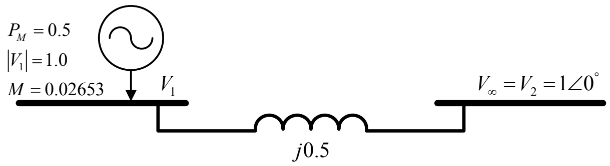

Fig. 8: Single Machine Infinite Bus System

TABLE VII
ANALOG HARDWARE INTERVALS

Component	Parameter	Interval
Generator	**Terminal Voltage**	[-10,10]V
Transmission Line	Current	[-300,300]uA
	Reactance	[10, 500]kΩ
Generator	Input Power	[-10,10]V
	Angle	[-10,10]V
	Angular Velocity	[-25, 25]mV
	Angular Acceleration	[-25, 25]mV

TABLE VIII
POWER SYSTEM INTERVALS

Component	Parameter	Interval
Generator	**Terminal Voltage**	[1,1]*
Transmission Line	Current	[-3.0,3.0]
	Reactance	[0.5,0.5]*
Generator	Input Power	[0.5,0.5]*
	Angle (radians)	[0.166,0.334]
	Angular Velocity	[-.745,.745]
	Angular Acceleration	[-6.36,6.36]

*These are thin intervals since there is only one reactance value (one line) and the input power/terminal voltage do not change for this case.

The time scaling factor was set to $\tau = 4945$ and k_V and k_4 were set at 5 to ensure a very fast simulation and high signal-to-noise ratio for voltages. The other scaling factors were then chosen heuristically to satisfy the specified constraints. The values chosen were: k_I=.0001, m=k_1=k_5=.0001, k_2=250, k_3=192000 and α=1. The configured analog hardware was simulated to verify proper scaling. Table IX details the levels seen in this simulation. All the values are within the specified hardware intervals. In addition, when compared to the unscaled system is consistent with the magnitude and time scaling with negligible error. Errors are expected for large perturbations due to linear approximations made when determining the power system intervals. This example considered a single disturbance. Monte Carlo analysis could be used to develop a large set of initial conditions and disturbances for developing the power system intervals.

TABLE IX
ANALOG HARDWARE SIMULATION INTERVALS

Component	Parameter	Interval
Generator	**Terminal Voltage**	[0,5]V
Transmission Line	Current	[16.5,98.6]uA
	Reactance	[50, 50]kΩ
Generator	Input Power	[0.5,0.5]V
	Angle	[.167,.340]V
	Angular Velocity	[-19, 19]mV
	Angular Acceleration	[-4.2, 4.2]mV

VI. CONCLUSION

The configuration method proposed in this paper determines analog hardware gains along with magnitude and time scaling parameters to ensure the analog hardware properly emulates the power system under study. With remote control of the hardware this configuration process can be automated via software. Linearized analysis determined power system intervals and a heuristic approach was taken to determine the scaling factors and gains based on this and the analog hardware intervals. This process can be implemented in an optimization scheme to minimize power dissipation of the analog hardware or other objective functions. Overall this paper contributes a systematic approach to configuring an analog computer based on analysis of the system under study.

REFERENCES

[1] L. J. Lane, "A Method of Scaling and Checking Computer Circuits," *Transactions of the American Institute of Electrical Engineers: Part II: Applications and Industry,* vol. 77, pp. 67-70, 1958.

[2] B. Murphy, "A Recommended Preparation Programming and Verification Procedure of Universal Applicability to General Purpose Electronic Analog Computers," *Proceedings of the 2nd International Analogue Computation Meeting,* pp. 200-204, 1959.

[3] J. R. Ashley, *Introduction to Analog Computation*: John Wiley and Sons, Inc., 1963.

[4] C. A. A. Wass and K. C. Garner, *Introduction to Electronic Analogue Computers*, 2nd ed.: Pergamon Press Ltd., 1965.

[5] V. P. Kodali, "A Study of the Applications of Analog Computers," *IEEE Transactions on Industrial Electronics and Control Instrumentation,* vol. IECI-14, pp. 1-7, April 1967 1967.

[6] R. Fried, R. S. Cherkaoui, C. C. Enz, A. Germond, and E. A. Vittoz, "Approaches for analog VLSI simulation of the transient stability of large power networks," *IEEE Transactions on Circuits and Systems I-Fundamental Theory and Applications,* vol. 46, pp. 1249-1263, OCT 1999.

[7] J. Yakaski, Q. Lui, and C. Nwankpa, "Analog Emulation Using a Reconfigurable Classical Generator Model for Load Flow Analysis," *Proceedings of Power Systems Computation Conference (PSCC),* 2005.

[8] A. St.Leger and C. O. Nwankpa, "Reconfigurable Transmission Line Model for Analog Power Flow Computation," *Proceedings of the 15th Power Systems Computation Conference (PSCC),* 2005.

[9] A. Deese and C. O. Nwankpa, "Emulation of Power System Load Dynamic Behavior Through Reconfigurable Analog Circuits," *International Symposium on Circuits and Systems (ISCAS),* pp. 1691-1694, 2006.

[10] N. Semiconductor, "LM13700 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers," 2000 http://www.national.com.

[11] C. O. Nwankpa, S. M. Shahidehpour, and Z. Schuss, "A Stochastic Approach to small Disturbance Stability Analysis," *IEEE Proceedings of Power Systems,* vol. 7, pp. 1519-1528, November 1992 1992.

[12] A. R. Bergen and D. J. Hill, "A Structure Preserving Model for Power System Stability Analysis," *IEEE Transactions on Power Apparatus and Systems,* vol. 100, pp. 25-35, 1981.